IN THE CLAIMS

Claims 24-39 and 42-51 are pending in this application. Please amend claim 50 as follows:

1-23. (cancelled)

24. (original) A semiconductor device formed on one semiconductor substrate, comprising:

a first word line;

a second word line;

a read bit line;

a first write bit line;

a first memory cell connected to the first and second word lines, the read bit line and the first write bit line;

a third word line;

a first bit line;

a second bit line; and

a second memory cell connected to the third word line, the first bit line and the second bit line,

wherein the first memory cell includes a first inverter circuit, a second inverter circuit having an input connected to an output of the first inverter circuit and an output connected to an input of the first inverter circuit, a first transistor having a source-drain path one of which is connected to the read bit line, a second transistor having a source-drain path connected to a first terminal, one of which is connected to the other of the source-drain path and the other of which is supplied with a first voltage, and a third transistor having a source-drain path one of which is connected to the input of the first inverter circuit and the other of which is connected to the first write bit line,

wherein a gate of the fist transistor is connected to the first word line,

wherein a gate of the second transistor is connected to the output of the first inverter circuit,

wherein a gate of the third transistor is connected to the second word line, and

wherein the second memory cell includes a third inverter circuit, a fourth inverter circuit having an input connected to an output of the third inverter circuit and an output connected to an input of the third inverter circuit, a fourth transistor having

a source-drain path connected between the first bit line and the output of the third inverter circuit, and a gate connected to the third word line, and a fifth transistor having a source-drain path connected to the second bit line and the input of the third inverter circuit, and a gate connected to the third word line.

25. (original) The semiconductor device according to claim 24, wherein the first voltage is a ground potential.

26. (original) The semiconductor device according to claim 24, wherein each of the first through fourth inverter circuits includes one P type MOS transistor and one N type MOS transistor.

27. (original) The semiconductor device according to claim 24,

wherein the first bit line and the second bit line are respectively bit lines commonly used for writing and reading,

wherein the first word line is a word line used for read only,

wherein the second word line is a word line used for write only, and

wherein the third word line is a word line commonly used in writing and reading.

28. (original) The semiconductor device according to claim 24,

wherein the first memory cell is a multi-port memory cell,

wherein the second memory cell is a one-port memory cell,

wherein said semiconductor device includes a plurality of multi-port memory cells and a plurality of one-port memory cells, and

wherein the plural one-port memory cells are larger than the plural multi-port memory cells in memory capacity.

29. (original) The semiconductor device according to claim 28, wherein the first memory cell is a two-port memory cell.

30. (original) The semiconductor device according to claim 24, further including a second write bit line,

wherein the first memory cell further includes a sixth transistor having a source-drain path one of which is connected to the output of the first inverter circuit and the other of which is connected to the second write bit line, and a gate connected to the second word line.

31. (original) A semiconductor device formed on one semiconductor substrate, comprising:

a first word line;

a second word line;

a read bit line;

a first write bit line;

a first memory cell connected to the first and second word lines, the read bit line and the first write bit line;

a third word line;

a first bit line;

a second bit line; and

a second memory cell connected to the third word line, and the first bit line and the second bit line,

wherein the first memory cell includes:

a latch circuit including a first inverter circuit, and a second inverter circuit having an input connected to an output of the first inverter circuit and an output connected to an input of the first inverter circuit;

a first and a second transistors whose source-drain paths are series-connected between the read bit line and a first terminal supplied with a first voltage; and

a third transistor having a source-drain path connected between the latch circuit and the first write bit line and a gate connected to the second word line,

wherein a gate of the first transistor is connected to the first word line,

wherein a gate of the second transistor is connected to the latch circuit, and

wherein the second memory cell includes a third inverter circuit, a fourth inverter circuit having an input connected to an output of the third inverter circuit, and an output connected to an input of the third inverter circuit, a fourth transistor having a source-drain path connected to the first bit line and the output of the third inverter circuit, and a gate connected to the third word line, and a fifth transistor having a

source-drain path connected to the second bit line and the input of the third inverter circuit, and a gate connected to the third word line.

32. (original) The semiconductor device according to claim 31,

wherein one of the source-drain path of the first transistor is connected to the read bit line, and the source-drain path of the second transistor is connected between the other of the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the input of the first inverter circuit and the first write bit line.

33. (original) The semiconductor device according to claim 31,

wherein one of the source-drain path of the first transistor is connected to the read bit line,

wherein the source-drain path of the second transistor is connected between the other of the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the output of the first inverter circuit and the first write bit line.

34. (original) The semiconductor device according to claim 31, wherein the first voltage is a ground potential.

35. (original) The semiconductor device according to claim 31,

wherein each of the first through fourth inverter circuits includes one P type MOS transistor and one N type MOS transistor.

36. (original) The semiconductor device according to claim 31,

wherein the first bit line and the second bit line are respectively bit lines commonly used for writing and reading,

wherein the first word line is a word line used for read only,

wherein the second word line is a word line used for write only, and

wherein the third word line is a word line commonly used in writing and reading.

37. (original) The semiconductor device according to claim 31,

wherein the first memory cell is a multi-port memory cell,

wherein the second memory cell is a one-port memory cell,

wherein said semiconductor device includes a plurality of multi-port memory cells and a plurality of one-port memory cells, and

wherein the plural one-port memory cells are larger than the plural multi-port memory cells in memory capacity.

38. (original) The semiconductor device according to claim 37, wherein the first memory cell is a two-port memory cell.

39. (original) The semiconductor device according to claim 31, further including a second write bit line,

wherein the first memory cell further includes a sixth transistor having a source-drain path connected between the output of the first inverter circuit and the second write bit line, and a gate connected to the second word line,

wherein one of the source-drain path of the first transistor is connected to the read bit line,

wherein the source-drain path of the second transistor is connected between the other of the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the input of the first inverter circuit and the first write bit line.

40-41. (cancelled)

42. (original) A semiconductor device formed on one semiconductor substrate, comprising:

a first word line;

a second word line;

a read bit line;

a first write bit line;

a first memory cell connected to the first and second word lines, the read bit line and the first write bit line;

a third word line;

a first bit line; and

a second memory cell connected to the third word line and the first bit line,

wherein the first memory cell includes:

a latch circuit including a first inverter circuit, and a second inverter circuit having an input connected to an output of the first inverter circuit and an output connected to an input of the first inverter circuit;

a first and a second transistors whose source-drain paths are series-connected between the read bit line and a first terminal supplied with a first voltage; and

a third transistor having a source-drain path connected between the latch circuit and the first write bit line and a gate connected to the second word line,

wherein a gate of the first transistor is connected to the first word line,

wherein a gate of the second transistor is connected to the latch circuit, and

wherein the second memory cell includes a fourth transistor having a gate connected to the third word line and a source-drain path whose one is connected to the first bit line, and a capacitor having a pair of electrodes one of which is connected to the other of the source-drain path of the fourth transistor and the other of which is supplied with a second voltage.

43. (original) The semiconductor device according to claim 42,

wherein one of the source-drain path of the first transistor is connected to the read bit line,

wherein the source-drain path of the second transistor is connected between the other of the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the input of the first inverter circuit and the first write bit line.

44. (original) The semiconductor device according to claim 42,

wherein one of the source-drain path of the first transistor is connected to the read bit line,

wherein the source-drain path of the second transistor is connected between the other of the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the output of the first inverter circuit and the first write bit line.

45. (original) The semiconductor device according to claim 42,

wherein the first voltage is a ground potential, and

wherein the second voltage is a plate potential larger than the ground potential.

46. (original) The semiconductor device according to claim 42, wherein each of the first through fourth inverter circuits includes one P type MOS transistor and one N type MOS transistor.

47. (original) The semiconductor device according to claim 42,

wherein the first bit line and the second bit line are respectively bit lines commonly used for writing and reading,

wherein the first word line is a word line used for read only,

wherein the second word line is a word line used for write only, and

wherein the third word line is a word line commonly used in writing and reading.

48. (original) The semiconductor device according to claim 42,

wherein the first memory cell is a multi-port memory cell,

wherein the second memory cell is a one-port memory cell,

wherein said semiconductor device includes a plurality of multi-port memory cells and a plurality of one-port memory cells, and

wherein the plural one-port memory cells are larger than the plural multi-port memory cells in memory capacity.

49. (original) The semiconductor device according to claim 48, wherein the first memory cell is a two-port memory cell.

50. (currently amended) The semiconductor device according to claim 42, further including a second write bit line,

wherein the first memory further includes a fifth transistor having a source-drain path ~~on eof~~ one of which is connected to the output of the inverter circuit and the other of which is connected to the second write bit line, and a gate connected to the second word line,

wherein the input of the first inverter circuit is connected to the output of the second inverter circuit,

wherein the output of the first inverter circuit is connected to the input of the first inverter circuit,

wherein one of the source-drain path of the first transistor is connected to the read bit line,

wherein the source-drain path of the second transistor is connected between the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the output of the second inverter circuit and the first write bit line.

51. (original) The semiconductor device according to claim 42, wherein the first through fourth transistors are respectively N channel type MOS transistors.